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FSDM07652R

Green Mode Fairchild Power Switch (FPS^{TM})

Features

- Internal Avalanche Rugged Sense FET
- Advanced Burst-Mode operation consumes under 1 W at 240VAC & 0.5W load
- Precision Fixed Operating Frequency (66kHz)
- Internal Start-up Circuit
- Pulse by Pulse Current Limiting
- Abnormal Over Current Protection (AOCP)
- Over Voltage Protection (OVP)
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under Voltage Lock Out (UVLO) with hysteresis
- Low Operating Current (2.5mA)
- Built-in Soft Start

Application

- SMPS for LCD monitor and STB
- Adaptor

Description

The FSDM07652R is an integrated Pulse Width Modulator (PWM) and Sense FET specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high voltage power switching regulator which combine an avalanche rugged Sense FET with a current mode PWM control block. The PWM controller includes integrated fixed frequency oscillator, under voltage lockout, leading edge blanking (LEB), optimized gate driver, internal soft start, temperature compensated precise current sources for a loop compensation and self protection circuitry. Compared with discrete MOSFET and PWM controller solution, it can reduce total cost, component count, size and weight simultaneously increasing efficiency, productivity, and system reliability. This device is a basic platform well suited for cost effective designs of flyback converters.

OUTPUT POWER TABLE

PRODUCT	230VAC ±15%[3]		85-265VAC	
	Adapter[1]	Open Frame[2]	Adapter[1]	Open Frame[2]
FSDM0565R	60W	70W	50W	60W
FSDM07652R	70W	80W	60W	70W

Table 1. Notes: 1. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient. 2. Maximum practical continuous power in an open frame design at 50°C ambient. 3. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

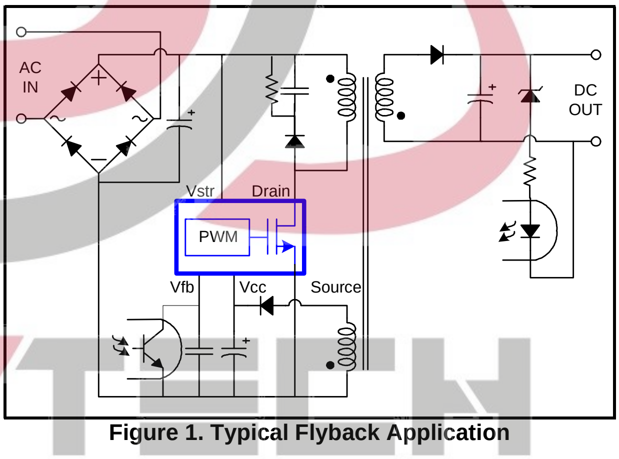


Figure 1. Typical Flyback Application

Internal Block Diagram

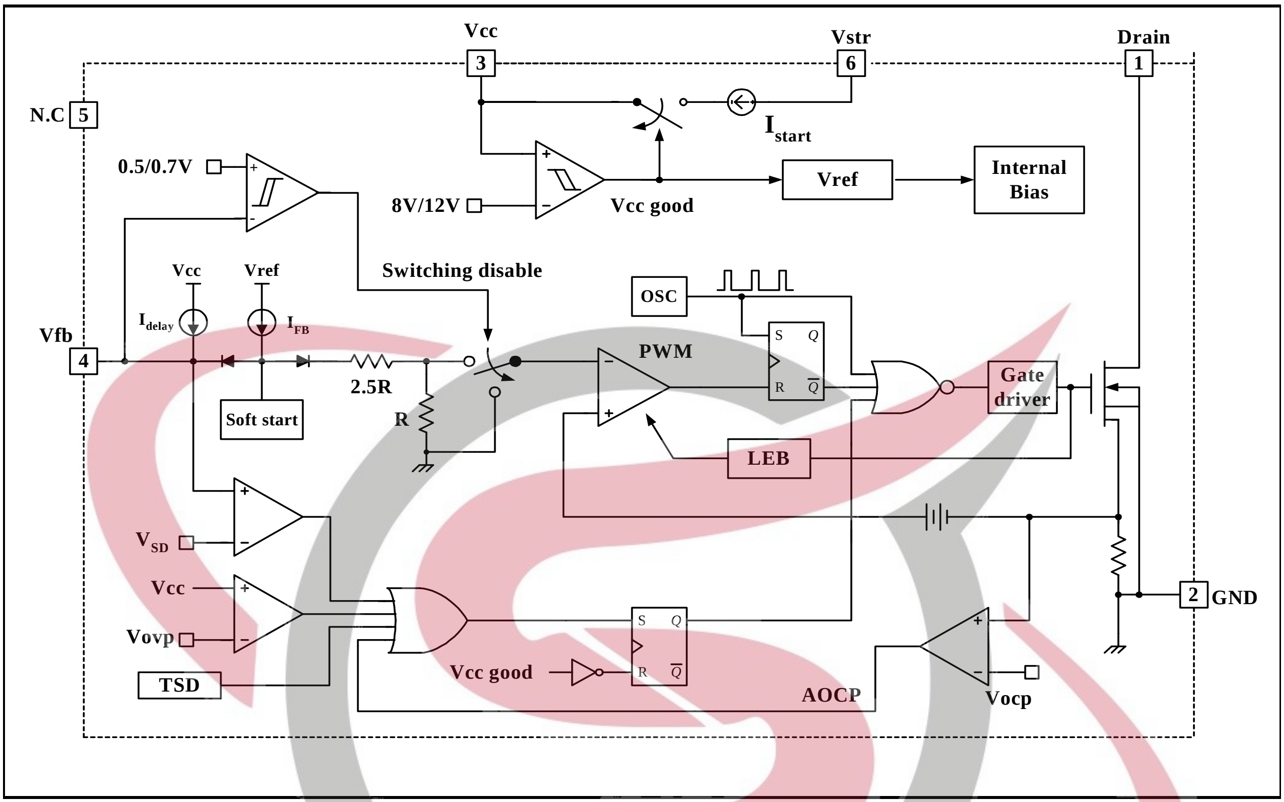


Figure 2. Functional Block Diagram of FSDM07652R

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Drain	This pin is the high voltage power Sense FET drain. It is designed to drive the transformer directly.
2	GND	This pin is the control ground and the Sense FET source.
3	Vcc	This pin is the positive supply voltage input. During start up, the power is supplied by an internal high voltage current source that is connected to the Vstr pin. When Vcc reaches 12V, the internal high voltage current source is disabled and the power is supplied from the auxiliary transformer winding.
4	Vfb	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6.0V, the over load protection is activated resulting in shutdown of the FPS^{TM}.
5	N.C	-
6	Vstr	This pin is connected directly to the high voltage DC link. At startup, the internal high voltage current source supplies internal bias and charges the external capacitor that is connected to the Vcc pin. Once Vcc reaches 12V, the internal current source is disabled.

Pin Configuration

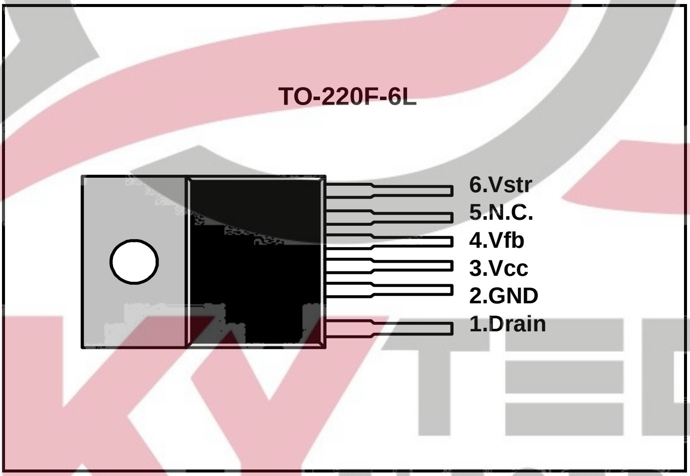


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DSS}	650	V
Vstr Max Voltage	V_{STR}	650	V
Pulsed Drain current (Tc=25°C)(1)	I_{DM}	15	A_{DC}
Continuous Drain Current(Tc=25°C)	I_D	3.8	A
Continuous Drain Current(Tc=100°C)		2.4	A
Single pulsed avalanche energy (2)	E_{AS}	370	mJ
Single pulsed avalanche current (3)	I_{AS}	-	A
Supply voltage	V_{CC}	20	V
Input voltage range	V_{FB}	-0.3 to V_{CC}	V
Total power dissipation(Tc=25°C)	P_D(Watt H/S)	45	W
Operating junction temperature	T_j	Internally limited	°C
Operating ambient temperature	T_A	-25 to +85	°C
Storage temperature range	T_{STG}	-55 to +150	°C
ESD Capability, HBM Model (All pins excepts for Vstr and Vfb)	-	2.0 (GND-Vstr/Vfb=1.5kV)	kV
ESD Capability, Machine Model (All pins excepts for Vstr and Vfb)	-	300 (GND-Vstr/Vfb=225V)	V

Notes:

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L=14mH, starting Tj=25°C
3. L=13uH, starting Tj=25°C

Thermal Impedance

Parameter	Symbol	Value	Unit
Junction-to-Ambient Thermal	θ_{JA}(1)	49.90	°C/W
Junction-to-Case Thermal	θ_{JC}(2)	2.78	°C/W

Notes:

1. Free standing with no heat-sink under natural convection.
2. Infinite cooling condition - Refer to the SEMI G30-88.

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET SECTION						
Drain source breakdown voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V	-	-	50	μA
		V_{DS}= 520V V_{GS} = 0V, T_C = 125°C	-	-	200	μA
Static drain source on resistance (1)	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	-	1.4	1.6	Ω
Output capacitance	C_{OSS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	-	100	-	pF
Turn on delay time	$T_{D(ON)}$	V_{DD}= 325V, I_D= 5A (MOSFET switching time is essentially independent of operating temperature)	-	22	-	ns
Rise time	T_R		-	60	-	
Turn off delay time	$T_{D(OFF)}$		-	115	-	
Fall time	T_F		-	65	-	
CONTROL SECTION						
Initial frequency	F_{OSC}	V_{FB} = 3V	60	66	72	kHz
Voltage stability	F_{STABLE}	13V ≤ Vcc ≤ 18V	0	1	3	%
Temperature stability (2)	ΔF_{OSC}	-25°C ≤ Ta ≤ 85°C	0	±5	±10	%
Maximum duty cycle	D_{MAX}	-	75	80	85	%
Minimum duty cycle	D_{MIN}	-	-	-	0	%
Start threshold voltage	V_{START}	V_{FB}=GND	11	12	13	V
Stop threshold voltage	V_{STOP}	V_{FB}=GND	7	8	9	V
Feedback source current	I_{FB}	V_{FB}=GND	0.7	0.9	1.1	mA
Soft-start time	T_S	V_{FB}=3	-	10	15	ms
Leading Edge Blanking time	T_{LEB}	-	-	250	-	ns
BURST MODE SECTION						
Burst Mode Voltages (2)	V_{BURH}	Vcc=14V	-	0.7	-	V
	V_{BURL}	Vcc=14V	-	0.5	-	V
PROTECTION SECTION						
Peak current limit (4)	I_{OVER}	V_{FB}=5V, V_{CC}=14V	2.2	2.5	2.8	A
Over voltage protection	V_{OVP}	-	18	19	20	V
Abnormal Over current protection current (3)	I_{AOCP}	-	5.54	6.15	6.77	A
Thermal shutdown temperature (2)	T_{SD}		130	145	160	°C
Shutdown feedback voltage	V_{SD}	V_{FB} ≥ 5.5V	5.5	6.0	6.5	V

Shutdown delay current	I_{DELAY}	V_{FB}=5V	2.8	3.5	4.2	µA
TOTAL DEVICE SECTION						
Operating supply current (5)	I_{OP}	V_{FB}=GND, V_{CC}=14V	-	2.5	5	mA
	$I_{OP(MIN)}$	V_{FB}=GND, V_{CC}=10V				
	$I_{OP(MAX)}$	V_{FB}=GND, V_{CC}=18V				

Notes:

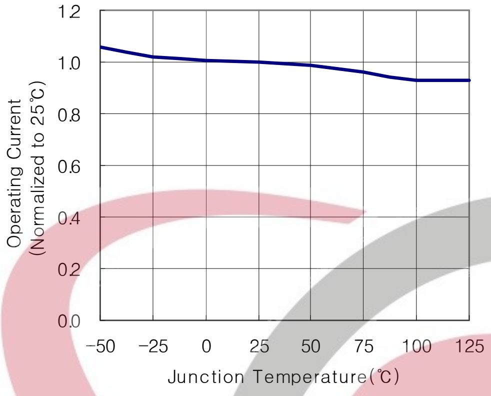
1. Pulse test : Pulse width ≤ 300µS, duty ≤ 2%
2. These parameters, although guaranteed at the design, are not tested in mass production.
3. These parameters, although guaranteed, are tested in EDS(wafer test) process.
4. These parameters indicate the inductor current.
5. This parameter is the current flowing into the control IC.

Comparison Between FS6M07652RTC and FSDM07652R

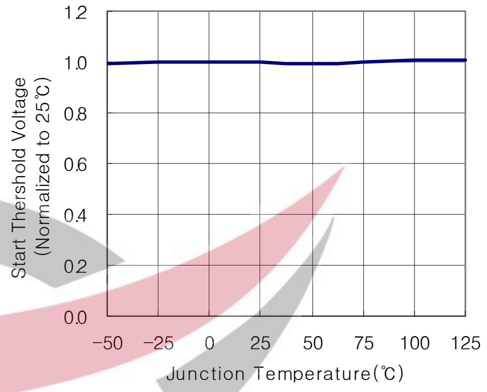
Function	FS6M07652RTC	FSDM07652R	FSDM07652R Advantages
Soft-Start	Adjustable soft-start time using an external capacitor	Internal soft-start with typically 10ms (fixed)	• Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
Burst Mode Operation	• Built into controller • Output voltage drops to around half	• Built into controller • Output voltage fixed	• Improve light load efficiency • Reduces no-load consumption

Typical Performance Characteristics

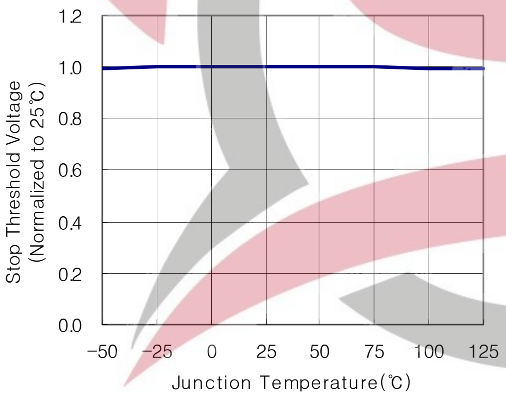
(These Characteristic Graphs are Normalized at Ta= 25°C)



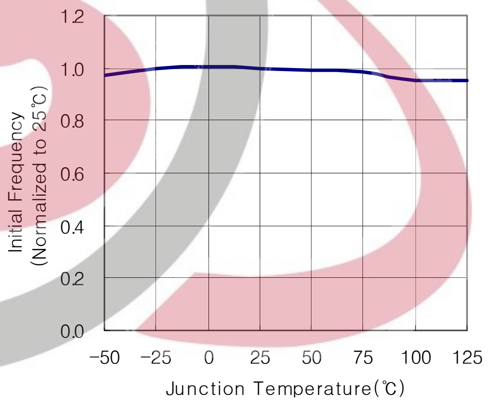
Operating Current vs. Temp



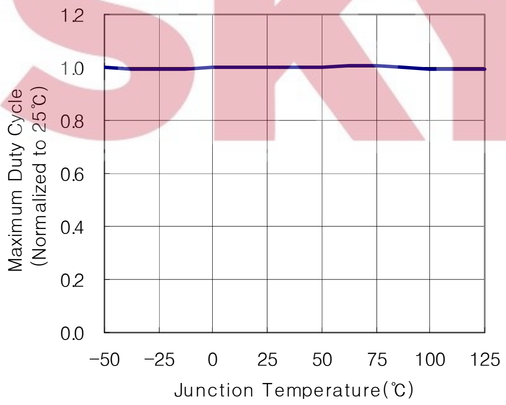
Start Threshold Voltage vs. Temp



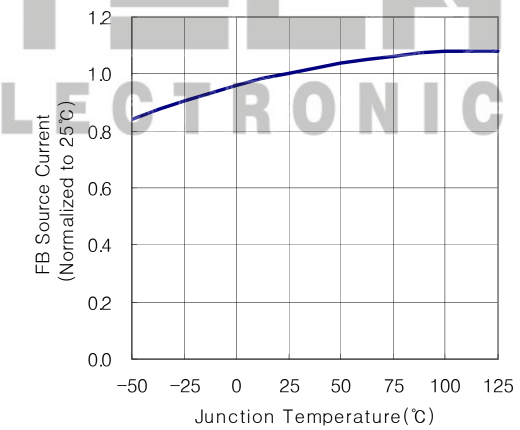
Stop Threshold Voltage vs. Temp



Operating Freqency vs. Temp



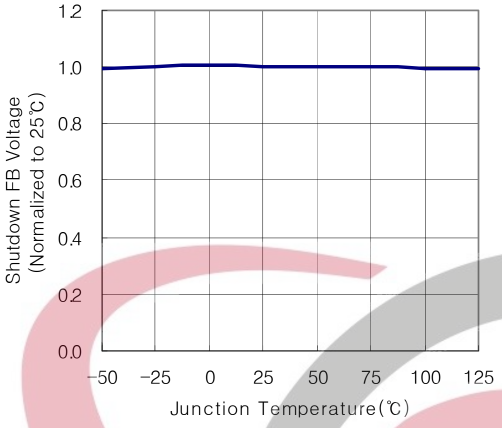
Maximum Duty vs. Temp



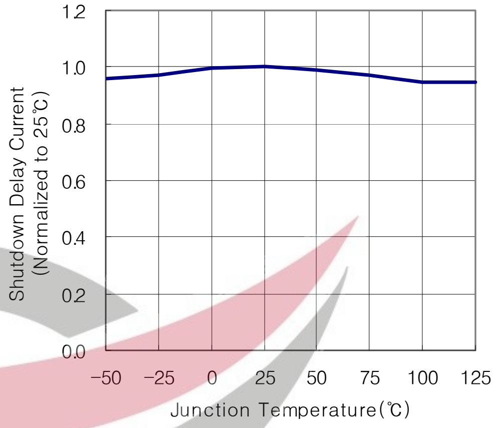
Feedback Source Current vs. Temp

Typical Performance Characteristics (Continued)

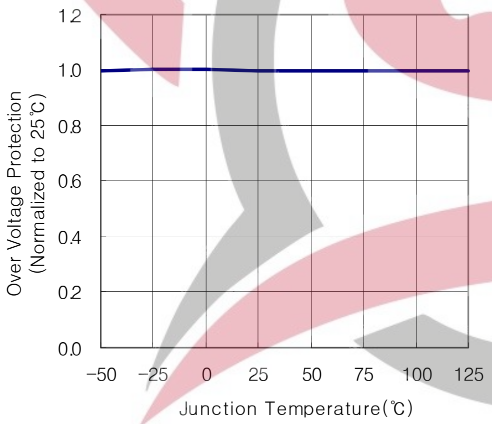
(These Characteristic Graphs are Normalized at Ta= 25°C)



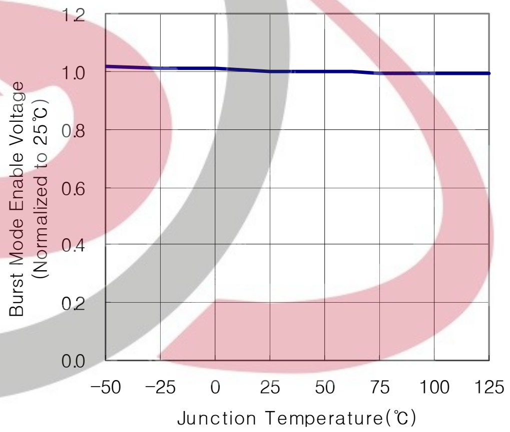
ShutDown Feedback Voltage vs. Temp



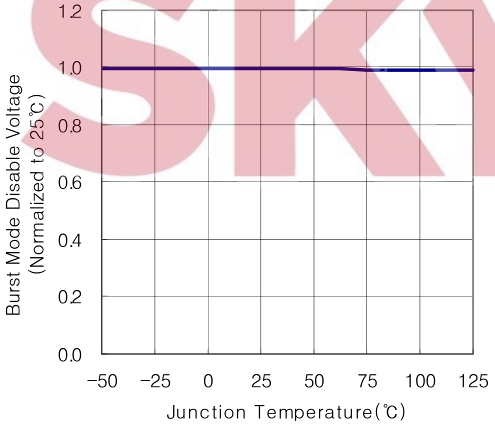
ShutDown Delay Current vs. Temp



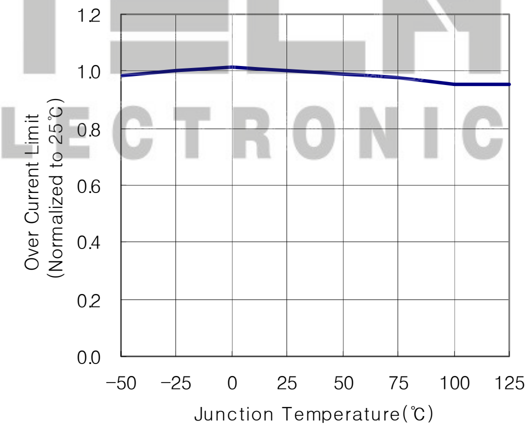
Over Voltage Protection vs. Temp



Burst Mode Enable Voltage vs. Temp



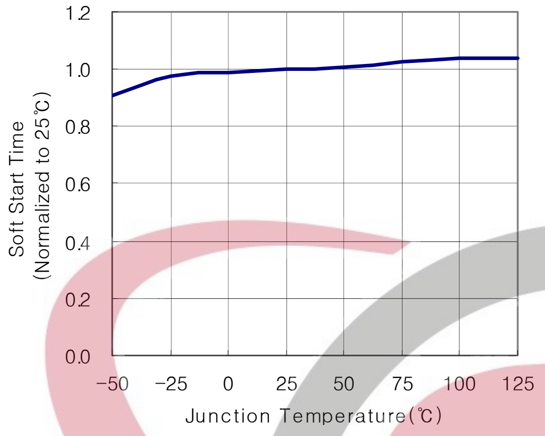
Burst Mode Disable Voltage vs. Temp



Current Limit vs. Temp

Typical Performance Characteristics (Continued)

(These Characteristic Graphs are Normalized at Ta= 25°C)



Soft Start Time vs. Temp

Functional Description

1. Startup : In previous generations of Fairchild Power Switches (FPS^{TM}) the Vcc pin had an external start-up resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source. At startup, an internal high voltage current source supplies the internal bias and charges the external capacitor (C_{VCC}) that is connected to the Vcc pin as illustrated in figure 4. When Vcc reaches 12V, the FPS^{TM} begins switching and the internal high voltage current source is disabled. Then, the FPS^{TM} continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless Vcc goes below the stop voltage of 8V.

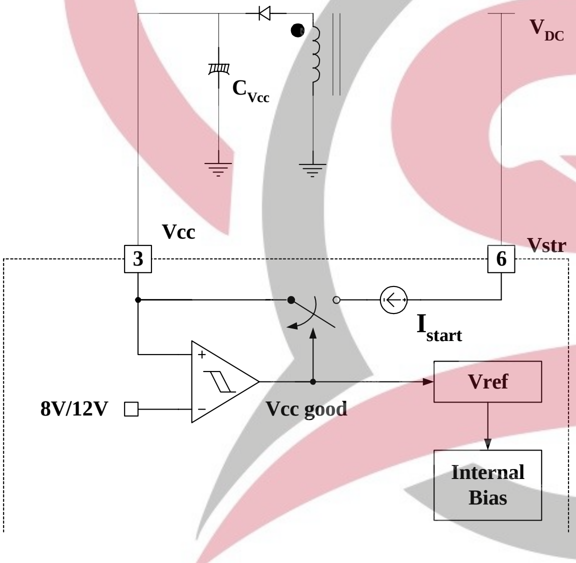


Figure 4. Internal startup circuit

2. Feedback Control : FSDM07652R employs current mode control, as shown in figure 5. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor plus an offset voltage makes it possible to control the switching duty cycle. When the reference pin voltage of the KA431 exceeds the internal reference voltage of 2.5V, the H11A817A LED current increases, thus pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-pulse current limit: Because current mode control is employed, the peak current through the Sense FET is limited by the inverting input of PWM comparator (Vfb*) as shown in figure 5. Assuming that the 0.9mA current source flows only through the internal resistor (2.5R +R= 2.8 kΩ), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (Vfb) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping Vfb*. Therefore, the peak value of the current through the Sense FET is limited.

2.2 Leading edge blanking (LEB) : At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the Rsense resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS^{TM} employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (T_{LEB}) after the Sense FET is turned on.

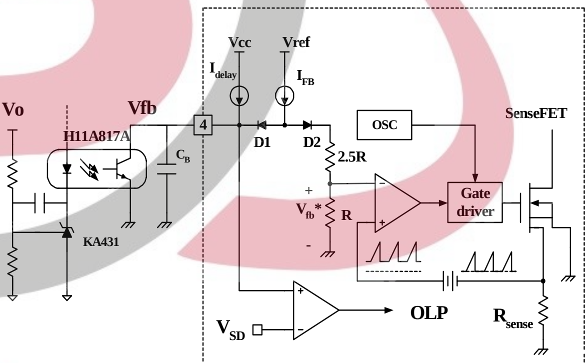


Figure 5. Pulse width modulation (PWM) circuit

3. Protection Circuit : The FSDM07652R has several self protective functions such as over load protection (OLP), abnormal over current protection (AOCP), over voltage protection (OVP) and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without increasing cost. Once the fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage, 8V, the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage,12V, the FPS^{TM} resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated (see figure 6).

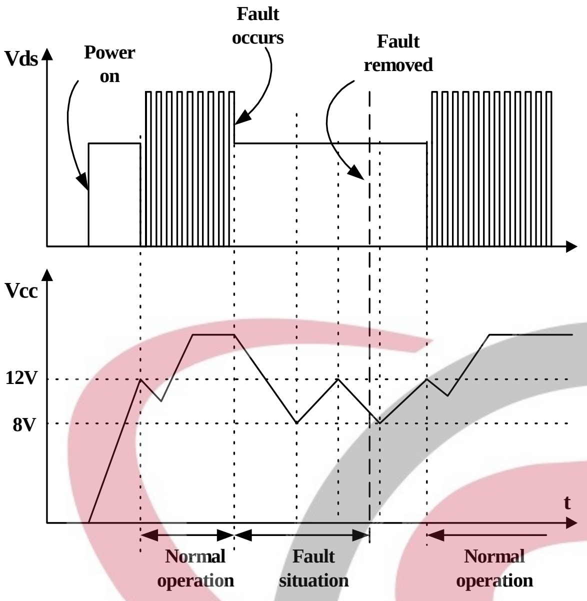


Figure 6. Auto restart operation

3.1 Over Load Protection (OLP) : Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is in the normal operation, the over load protection circuit can be activated during the load transition. In order to avoid this undesired operation, the over load protection circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the Sense FET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (Vfb). If Vfb exceeds 2.5V, D1 is blocked and the 3.5uA current source starts to charge C_B slowly up to Vcc. In this condition, Vfb continues increasing until it reaches 6V, when the switching operation is terminated as shown in figure 7. The delay time for shutdown is the time required to charge C_B from 2.5V to 6.0V with 3.5uA. In general, a 10 ~ 50 ms delay time is typical for most applications.

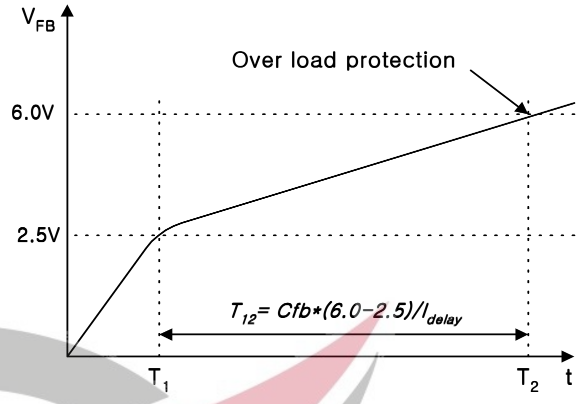


Figure 7. Over load protection

3.2 Abnormal Over Current Protection (AOCP) : Even though the FPS^{TM} has OLP (Over Load Protection) and current mode PWM feedback, these are not enough to protect the FPS^{TM} when a secondary side diode short or a transformer pin short occurs. The FPS^{TM} has an internal AOCP (Abnormal Over Current Protection) circuit as shown in figure 8. When the gate turn-on signal is applied to the power Sense FET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level for longer than 300ns, the reset signal is applied to the latch, resulting in the shutdown of SMPS.

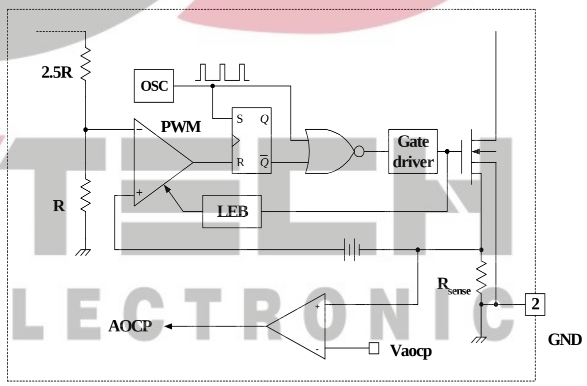


Figure 8. AOCP block

3.3 Over voltage Protection (OVP) : If the secondary side feedback circuit were to malfunction or a solder defect caused an open in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FPS^{TM} uses Vcc instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, an OVP circuit is activated resulting in the termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be designed to be below 19V.

3.4 Thermal Shutdown (TSD) : The Sense FET and the control IC are built in one package. This makes it easy for the control IC to detect the heat generation from the Sense FET. When the temperature exceeds approximately 150°C, the thermal shutdown is activated.

4. Soft Start : The FPS^{TM} has an internal soft start circuit that increases PWM comparator inverting input voltage together with the Sense FET current slowly after it starts up. The typical soft start time is 10msec, The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

5. Burst operation : In order to minimize power dissipation in standby mode, the FPS^{TM} enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in figure 9, the device automatically enters burst mode when the feedback voltage drops below V_{BURL}(500mV). At this point switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}(700mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in Standby mode.

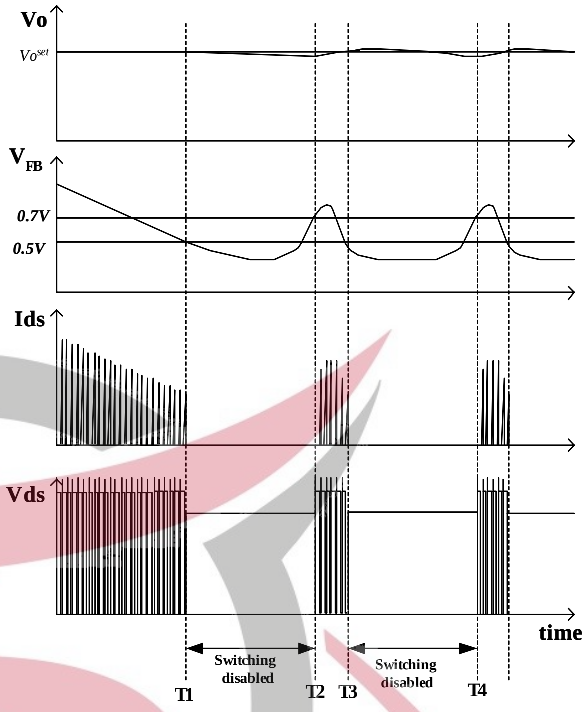


Figure 9. Waveforms of burst operation

Typical application circuit

Application	Output power	Input voltage	Output voltage (Max current)
LCD Monitor	40W	Universal input (85-265Vac)	5V (2.0A) 12V (2.5A)

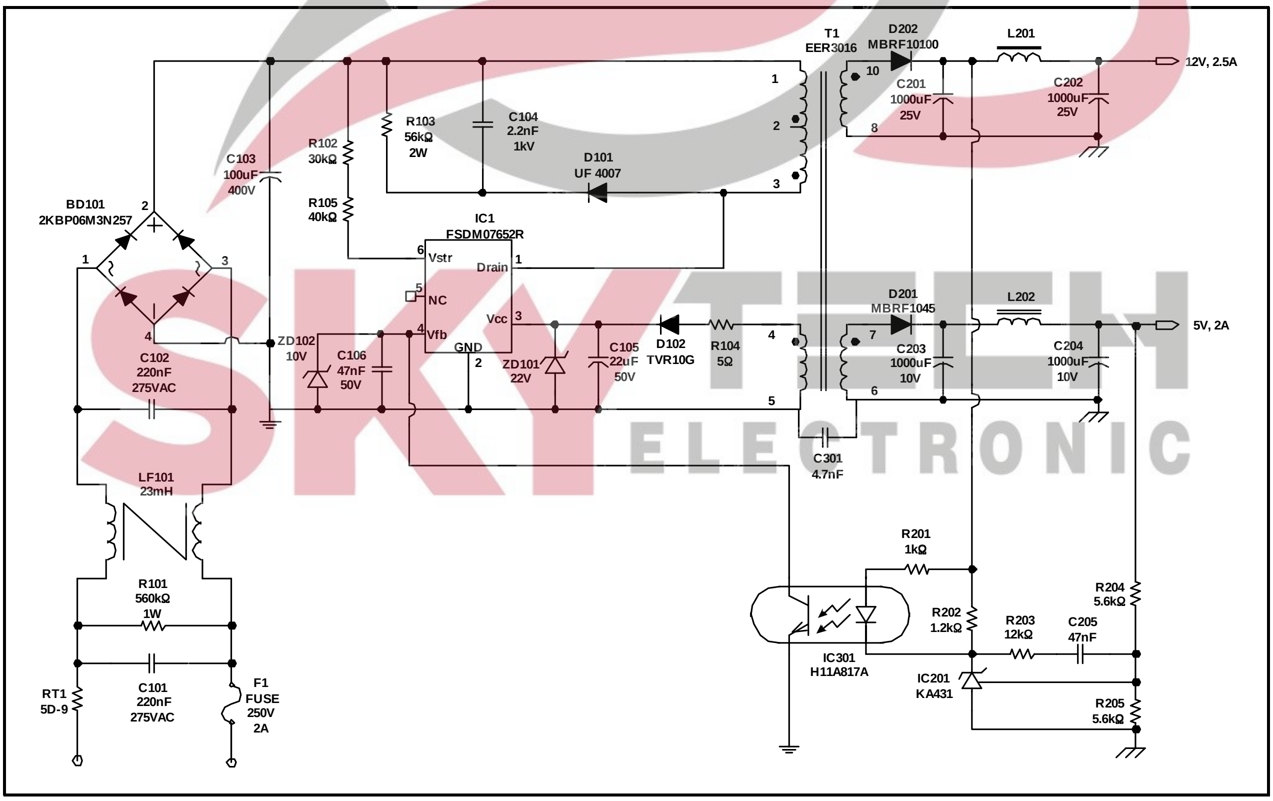
Features

- High efficiency (>81% at 85Vac input)
- Low zero load power consumption (<300mW at 240Vac input)
- Low standby mode power consumption (<800mW at 240Vac input and 0.3W load)
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (10ms)

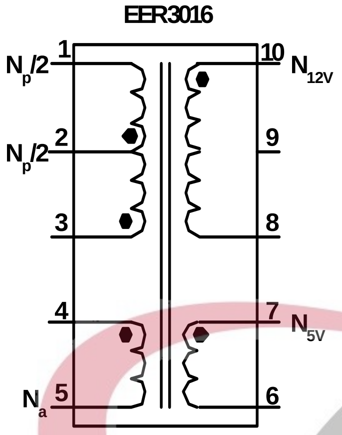
Key Design Notes

- Resistors R102 and R105 are employed to prevent start-up at low input voltage. After startup, there is no power loss in these resistors since the startup pin is internally disconnected after startup.
- The delay time for over load protection is designed to be about 50ms with C106 of 47nF. If a faster triggering of OLP is required, C106 can be reduced to 10nF.
- Zener diode ZD102 is used for a safety test such as UL. When the drain pin and feedback pin are shorted, the zener diode fails and remains short, which causes the fuse (F1) blown and prevents explosion of the opto-coupler (IC301). This zener diode also increases the immunity against line surge.

1. Schematic



2. Transformer Schematic Diagram



3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Na	4 → 5	$0.2^{\phi} \times 1$	8	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	2 → 1	$0.4^{\phi} \times 1$	18	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N12v	10 → 8	$0.3^{\phi} \times 3$	7	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N5v	7 → 6	$0.3^{\phi} \times 3$	3	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	3 → 2	$0.4^{\phi} \times 1$	18	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.050mm, 2Layers				

4.Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	520uH ± 10%	100kHz, 1V
Leakage Inductance	1 - 3	10uH Max	2nd all short

5. Core & Bobbin

Core : EER 3016
Bobbin : EER3016
Ae(mm2) : 96

6.Demo Circuit Part List

Part	Value	Note	Part	Value	Note
Fuse			C301	4.7nF	Polyester Film Cap.
F101	2A/250V				
NTC			**Inductor**		
RT101	5D-9		L201	5uH	Wire 1.2mm
Resistor			L202	5uH	Wire 1.2mm
R101	560K	1W			
R102	30K	1/4W			
R103	56K	2W			
R104	5	1/4W	**Diode**		
R105	40K	1/4W	D101	UF4007	
R201	1K	1/4W	D102	TVR10G	
R202	1.2K	1/4W	D201	MBRF1045	
R203	12K	1/4W	D202	MBRF10100	
R204	5.6K	1/4W	ZD101	Zener Diode	22V
R205	5.6K	1/4W	ZD102	Zener Diode	10V
			Bridge Diode		
			BD101	2KBP06M 3N257	Bridge Diode
Capacitor					
C101	220nF/275VAC	Box Capacitor	**Line Filter**		
C102	220nF/275VAC	Box Capacitor	LF101	23mH	Wire 0.4mm
C103	100uF/400V	Electrolytic Capacitor	**IC**		
C104	2.2nF/1kV	Ceramic Capacitor	IC101	FSDM07652R	FPS^{TM}(7A,650V)
C105	22uF/50V	Electrolytic Capacitor	IC201	KA431(TL431)	Voltage reference
C106	47nF/50V	Ceramic Capacitor	IC301	H11A817A	Opto-coupler
C201	1000uF/25V	Electrolytic Capacitor			
C202	1000uF/25V	Electrolytic Capacitor			
C203	1000uF/10V	Electrolytic Capacitor			
C204	1000uF/10V	Electrolytic Capacitor			
C205	47nF/50V	Ceramic Capacitor			

7. Layout

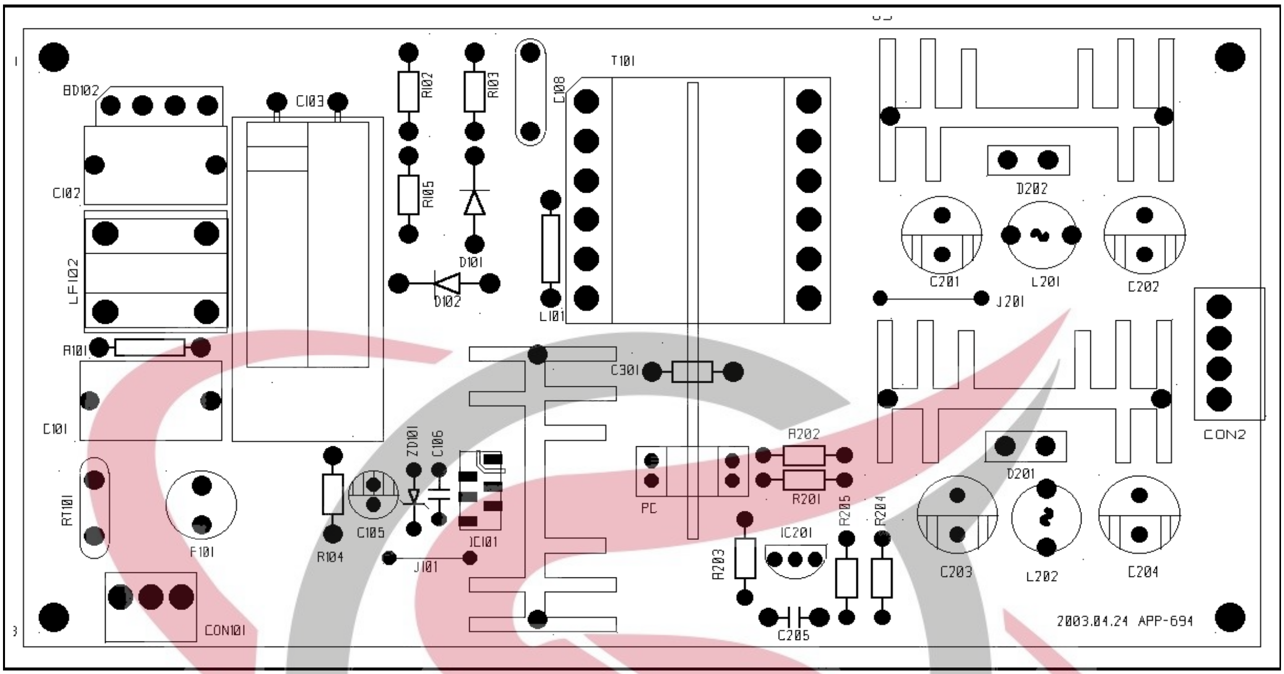


Figure 10. Layout Considerations for FSDM07652R

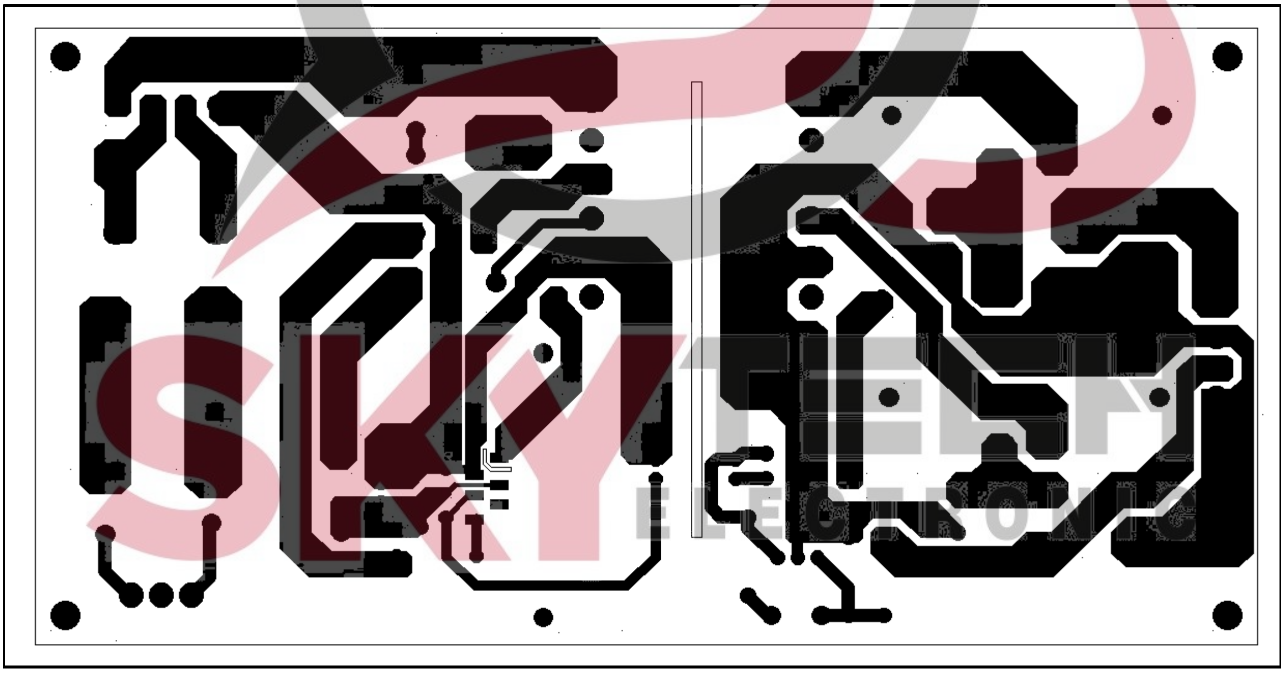
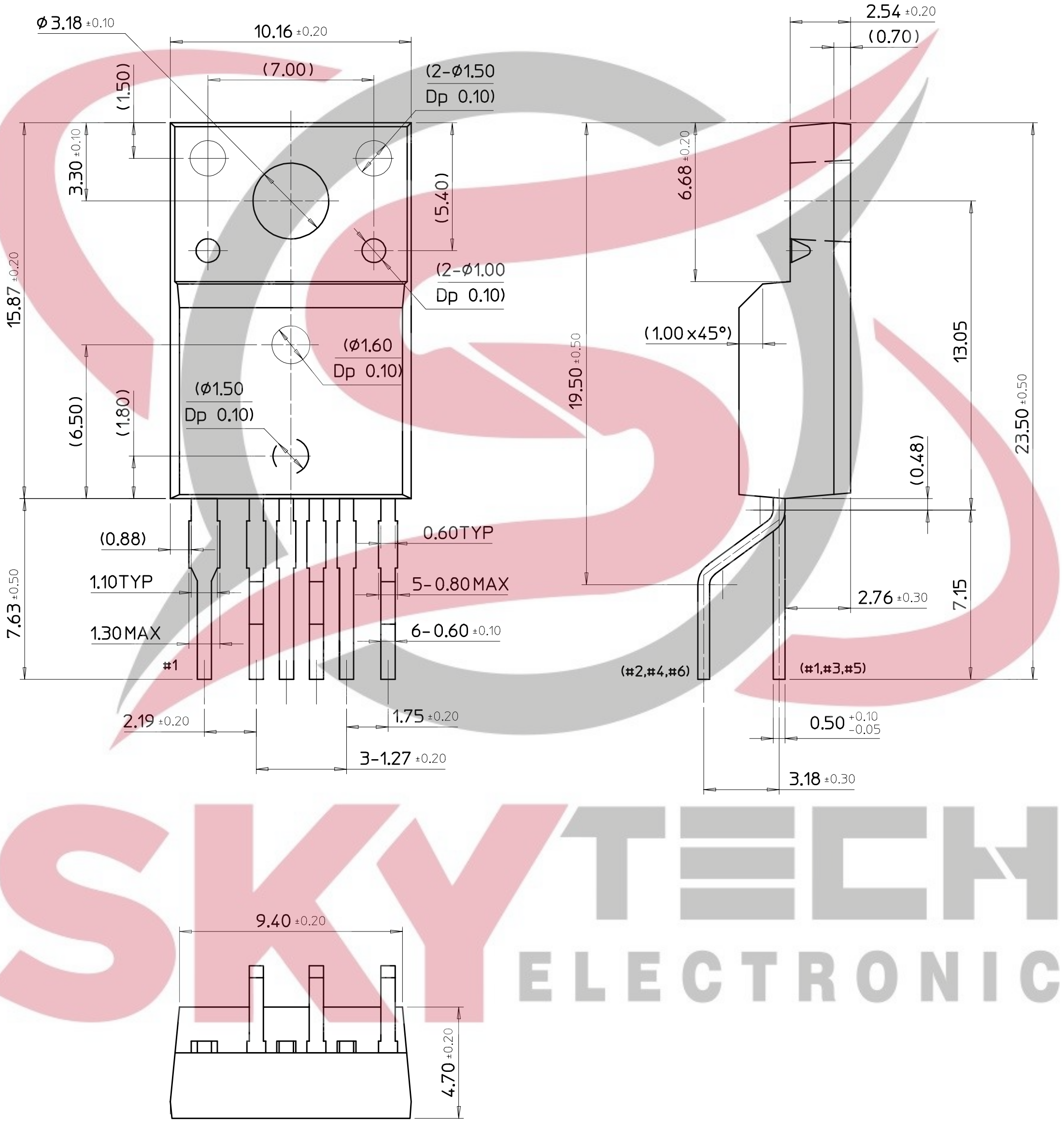


Figure 11. Layout Considerations for FSDM07652R

Package Dimensions

TO-220F-6L(Forming)



Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on)Max.
FSDM07652RWDTU	TO-220F-6L(Forming)	DM07652R	650V	1.6 Ω

WDTU : Forming Type

DISCLAIMER

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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